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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/557,454	04/24/2000	Lester J Kozlowski	98RSS367	7595
25700	7590	05/18/2005	EXAMINER	
FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691			JERABEK, KELLY L	
			ART UNIT	PAPER NUMBER
			2612	
			DATE MAILED: 05/18/2005	<i>12</i>

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/557,454	KOZLOWSKI ET AL.
	Examiner Kelly L. Jerabek	Art Unit 2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 07 March 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-12 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-4, 7-10 and 12 is/are rejected.

7) Claim(s) 5, 6 and 11 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "CMOS Imager Including a JFET Adapted to Detect Photons and Produce an Amplified Electrical Signal".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 4, 8, and 10 rejected under 35 U.S.C. 102(e) as being anticipated by Ishida et al. US 6,046,466.

Re claim 4, Ishida discloses in figures 1-7 an active pixel sensor supported on a substrate and used in digital photography (col. 1, lines 7-12; col. 15, lines 19-35). The active pixel sensor (120) includes a JFET (122) adapted to detect photons and produce an amplified electrical signal corresponding to the photons detected; and a readout switch transistor (123) coupled to a drain terminal of the JFET (122) (col. 15, line 51 – col. 16, line 38; col. 18, lines 8-23).

Re claims 8 and 10, see claim 4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida in view of Abramovich US 6,221,687.

Re claim 1, Ishida discloses in figures 1-7 an active pixel sensor supported on a substrate and used in digital photography (col. 1, lines 7-12; col. 15, lines 19-35). The device includes a silicon substrate (1201), a JFET (122) formed on a surface of the

silicon substrate and adapted to detect photons and produce an amplified electrical signal corresponding to the photons detected (col. 15, line 51 – col. 16, line 38; col. 18, lines 8-23). Although the Ishida reference discloses all of the above limitations it fails to distinctly disclose an overglass layer formed over the JFET to admit photons to the photo-absorbing layer of the JFET.

Abramovich discloses in figure 1A a solid state image sensor such as a CMOS. The image sensor (10) is formed on a semiconductor substrate and the image sensor (10) includes a glass packaging substrate (95) that allows light beams (85) to enter a photo-absorbing layer (col. 1, lines 25-40). Therefore, it would have been obvious for one skilled in the art to have been motivated to include a glass packaging substrate as disclosed by Abramovich in the active pixel sensor disclosed by Ishida. Doing so would provide a means for packaging and protecting an image sensor (Abramovich: col. 1, lines 38-41).

Re claim 9, see claim 1.

Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida in view of Abramovich and further in view of Reuss et al. US 5,618,688.

Re claim 2, the combination of the Ishida and Abramovich references discloses all of the limitations of claim 1 above. However, the combination does not specifically state that a JFET provides a relatively low corner frequency.

Reuss discloses in figures 1-4 an n-channel JFET. The JFET has a relatively low 1/f noise (corner frequency) (col. 7, lines 21-43). Therefore, it would have been obvious for one skilled in the art to have been motivated to include a JFET having a relatively low 1/f noise (corner frequency) as disclosed by Reuss in the active pixel sensor including a JFET as disclosed by Ishida in view of Abramovich. Doing so would provide a means for including a JFET having a low 1/f noise component in an active pixel sensor.

Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida in view of Abramovich and further in view of Reich et al. US 5,712,498.

Re claim 3, the combination of the Ishida and Abramovich references discloses all of the limitations of claim 1 above. However, the combination does not specifically state that an input referred noise of a JFET is relatively low.

Reich discloses a JFET readout amplifier employing a JFET feedback operation. The JFET readout amplifier yielded a relatively low input referred noise when the JFET operated with feedback (col. 8, lines 34-65). Therefore, it would have been obvious for one skilled in the art to have been motivated to include a JFET source-follower amplifier yielding a relatively low input referred noise as disclosed by Reich in the active pixel sensor including a JFET as disclosed by Ishida in view of Abramovich. Doing so would provide a means for including a JFET amplifier having a low input referred noise.

Claims 7 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida in view of Wurcer US 5,124,596.

Re claims 7 and 12, Ishida discloses all of the limitations of claims 4 and 10 above. However, the Ishida reference fails to distinctly state that the JFET is contained in a differential amplifier circuit.

Wurcer discloses a differential amplifier including JFET transistors. Wurcer states that JFET transistors are popular transistors for use in high quality differential transistors (col. 1, lines 15-38). Therefore, it would have been obvious for one skilled in the art to have been motivated to include a differential amplifier circuit including JFET transistors as disclosed by Wurcer in the active pixel sensor including a JFET as disclosed by Ishida. Doing so would provide a means for amplifying an electrical signal using a differential amplifier circuit consisting of JFET transistors.

Allowable Subject Matter

Claims 5-6 and 11 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fail to anticipate or render obvious the following technical features as recited in the highlighted claims:

Re claim 5, the prior art fails to teach or suggest "The CMOS APS pixel, wherein a source terminal of the readout switch transistor is connected to a bus and a resistor, forming a source follower circuit".

Re claim 6, the prior art fails to teach or suggest "The CMOS APS pixel further comprising: a first resistor connected between a gate terminal of the JFET and a drain terminal of the readout switch transistor; and a second resistor connected between a source terminal of the JFET and the drain terminal of the readout switch transistor, wherein the first and second resistors provide positive feedback and laser trimmability, and wherein a source terminal of the readout switch transistor is connected to a bus and a current source, forming a source follower".

Re claim 11, the prior art fails to teach or suggest: The digital camera as in claim 10, wherein a source terminal of the readout switch transistor is connected to a bus and a resistor, forming a source follower circuit".

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Isogai (US 5,528,059) discloses a photoelectric conversion device utilizing a JFET. The information regarding sensing incident light with a JFET is relevant material.

Isogai (US 5,847,381) discloses a photoelectric conversion apparatus having a light-shielding shunt line and a light-shielding shunt line and a light-shielding dummy line. The information regarding a JFET amplifier is relevant material.

Thompson (US 4,814,836) discloses a FET Photoconductor with a heterojunction in the channel. The information regarding an optically sensitive FET is relevant material.

Isogai (US 5,563,429) discloses a solid state imaging device. The information regarding a JFET amplifier is relevant material.

Shannon (US 3,721,839) discloses a solid state imaging device with an FET sensor. The information regarding employing FETs as sensors is relevant material.

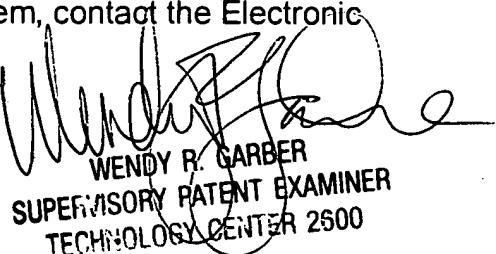
Brehmer et al. (US 6,130,423) discloses a method and apparatus for a CMOS image sensor with a distributed amplifier. The information regarding a CMOS image sensor is relevant material.

Contacts

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kelly L. Jerabek whose telephone number is **(571) 272-7312**. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on **(571) 272-7308**. The fax phone number for submitting all Official communications is 703-872-9306. The fax phone number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at **(571) 273-7312**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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